

JOURNAL OF TELECOMMUNICATIONS AND INFORMATION TECHNOLOGY

Preface

Despite the fact that a range of limitations are beginning to appear as CMOS technology is being raised to ever higher levels of perfection, it is anticipated that silicon will be the dominant material of the semiconductor industry for at least the first half of the 21st century. The forecast for microelectronics development published in 2001 by SIA (Semiconductor Industry Association) reaches ahead to the years 2010–2016. Moreover, a comparison with former SIA forecasts indicates that they become more aggressive (that is more optimistic) with time.

While the development of silicon microelectronics in the past could be attributed mostly to the reduction of the feature size (progress in lithography), today it relies more on new material solutions, such as SOI, SON, SiGe or SiC. The combination of this trend with continuous miniaturization provides the opportunity of improving IC functionality and speed of operation.

Telecommunications and information technology are arguably the most powerful drivers behind microelectronics product development nowadays. Thus plenty of new applications are being created for fast analog and RF circuits, as well as for information processing ones. It is clear that with the anticipated $f_{\max} = 130$ GHz and $f_T = 65$ GHz to be reached by RF bipolar transistors in 2005, according to the 2001 issue of ITRS (it is interesting to note that in 1999 ITRS predicted only $f_{\max} = 50$ GHz and $f_T = 40$ GHz for 2005), a lot of effort must be put into the development of appropriate material, processing, characterization and modeling. Such an outstanding progress, however, will not happen without increased speed offered by new materials solutions. SiGe-base HBTs may serve as an example here – a device with $f_T = 350$ GHz has already been reported in the literature.

High-speed isn't, however, everything. Portable wireless products push, for obvious reasons, for low-power solutions. This trend requires new architectural solutions (e.g., channel thinning), and in consequence, new material, such as SOI (or its possible successor SON – silicon-on-nothing), where current driveability is considerably higher than in conventional MOSFETs.

In this issue the Reader will find the second part of the papers and lectures presented during the 6th Symposium Diagnostics & Yield: Advanced Silicon Devices and Technologies for ULSI Era, which took place in Museum of Earth, Warsaw, Poland on June 22–25, 2003. A number of the papers are devoted to the most important issues concerning semiconductor technology (challenges faced by CMOS technology, gate-dielectric fabrication, wafer-cleaning problems, fabrication of nanostructures, micromachined sensors) and advanced materials, such as SOI and SiGe. Several papers address the problems of characterization of semiconductor structures and nanostructures (DC and noise analysis, photoelectric measurements, scanning probe microscopy), as well as those of IC testing and assembly. The subject of modeling (both devices and circuits) and parameter extraction is covered, too.

We hope the Readers will find these Proceedings useful and interesting.

Organization of this Symposium would not be possible without the support of Polish Committee for Scientific Research (research projects no. 4T11B03523, 8T11B07519, 8T11B07419). The organizers acknowledge also the contribution of the Committee of Electronics and Telecommunications of Polish Academy of Sciences, and the NEXUS Microsystems Association. The organizers are also grateful to the National Institute of Telecommunications for making this journal available for the publication of the Symposium papers.

Andrzej Jakubowski – General Chairman
Lidia Łukasiak – Programme Chairman
Guest Editors